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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/887,797	06/22/2001	Richard W. Adkisson	10012773-1	7649

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EXAMINER	
TORRES, JUAN A	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/887,797	ADKISSON, RICHARD W.	
	Examiner	Art Unit	
	Juan A. Torres	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-19* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

The indicated allowability of claims 1-19 is withdrawn in view of the newly discovered reference(s) to Kurd (US 6622255). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 14-16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), and further in view of Kurd (US 6622255).

As per claim 1 Price discloses a sampling compensation circuit operable to condition a SYNC pulse signal, wherein said SYNC pulse signal is based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals. Kurd discloses a jitter cycle delay compensation circuit coupled to said sampling compensation circuit, said jitter cycle delay

compensation circuit operating to tap said SYNC pulse signal after a predetermined delay based on a skew difference between said first and second clock signals (figure 6 column 5 lines 41-44). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18).

As per claim 2 Price also discloses a plurality of multiplexers arranged in series, each multiplexer operating to receive an input through a timing register associated (figure 11 column 12 lines 57-63).

As per claim 3 Price also discloses that the multiplexers are operable to insert a logic high condition in said SYNC pulse signal when said SYNC pulse signal is sampled to contain a plurality of logic lows during a predetermined time window (figure 11 column 12 line 63 to column 13 line7).

As per claim 14 Price (US 5450458) discloses sampling a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67); determining a clock state indicative of a phase difference between said first and second clock signals (figure 7 block 74 column 7 lines 46-48); Price doesn't disclose re-positioning the SYNC pulse signal based on said clock state and if the SYNC pulse

signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state. Kurt discloses re-positioning the SYNC pulse signal based on said clock state and if the SYNC pulse signal is out-of-phase by a predetermined amount with respect to said first clock signal, delaying said SYNC pulse signal based on said clock state (figure 5 column 5 lines 10-16). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18).

As per claim 15 Kurd also discloses adding at least an extra clock cycle when said clock state indicates that said first clock signal lags with respect to said second clock signal by a predetermined amount (figure 1 column 2 lines 44-46 column2 line 63 to column 5 line 5). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18).

As per claim 16 Kurd also discloses deleting at least an extra clock cycle when said clock state indicates that said second clock signal lags with respect to said first clock signal by a predetermined amount (figure 1 column 2 lines 46-48 column2 line 63

to column 5 line 5). Price and Kurd teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the delay system circuit disclosed by Kurd with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to synchronize the high rate transmission of data between different clock domains (Kurd column 1 lines 11-18).

As per claim 19 Price also discloses that the first and second clock signals comprise a core clock and a bus clock in a computer system (figure 7 blocks 58 and 82 column 9 lines 46-51 and 56-62)

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), further in view of Kurd (US 6622255) and further in view of Meagher (US 5054020). Price and Kurd disclose claim 2. Price and Kurd don't teach that the multiplexers operable to insert a [010] sequence in the SYNC pulse signal when the SYNC pulse signal is sampled to be all zeros during a predetermined time window. It is very well known and Meagher discloses to insert a [010] sequence the signal is sampled to be all zeros during a predetermined time window (figure 2, column 2 lines 30-31). Price, Kurd and Meagher teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate synchronization technique disclosed by Meagher with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined zeros (Meagher figure 2, column 2 lines 30-31).

Claims 5-9 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), further in view of Kurd (US 6622255), and further in view of Kim (US 6396322).

As per claim 5 Price and Kurd disclose claim 1. Price and Kurd don't teach that the jitter cycle delay compensation circuit with a series of delay registers, each operating to delay said SYNC pulse signal by a predetermined amount of time; and a multiplexer operable to select a delayed SYNC pulse output generated from said series of delay registers. Kim discloses a jitter cycle delay compensation circuit with a series of delay registers, each operating to delay said SYNC pulse signal by a predetermined amount of time, and a multiplexer operable to select a delayed SYNC pulse output generated from said series of delay registers (figure 6 page 3 paragraph [0032]). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]).

As per claim 6 Price, Kurd and Kim disclose claim 5. Kim also discloses that the series of delay registers comprises eight registers (Kim figure 6 page 3 paragraph [0032]).

As per claim 7 Price, Kurd and Kim disclose claim 5. Kurd also discloses a control signal generated by a state/correct block responsive to a skew difference between said first and second clock signals (Kurd figure 2 column 4 lines 25-29).

As per claim 8 Price, Kurd and Kim disclose claim 7 Kurd also discloses a state/correct block is coupled to a phase detector operating to detect said skew difference between said first and second clock signals (Kurd figure 1 block 108 column 2 lines 42-44).

As per claim 9 Price, Kurd and Kim disclose claim 7 Kim also discloses that control signal is stored in a flip-flop (Kim figure 6 page 3 paragraph [0032]).

As per claim 17 Price and Kurd teach claim 14. Price and Kurd didn't teach delaying by propagating said SYNC pulse signal through a series of delay registers operable to be selected by a multiplexer in response to a control signal corresponding to the clock state. Kim discloses a jitter cycle delay compensation circuit with a series of delay registers, each operating to delay said SYNC pulse signal by a predetermined amount of time, and a multiplexer operable to select a delayed SYNC pulse output generated from said series of delay registers (figure 6 page 3 paragraph [0032]). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number

of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]).

As per claim 18 Price, Kurd and Kim teach claim 17. Kim also discloses that control signal is stored in a flip-flop (Kim figure 6 page 3 paragraph [0032]). Price, Kurd and Kim teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the jitter compensation circuit disclosed by Kim with the SYNC pulse signal disclosed by Price and Kurd. The suggestion/motivation for doing so would have been to reduce the complexity of the jitter delay compensation unit, using only de pre-determinate number of delay elements that will eliminate the skew in a pre-determined number of cycles (Kim figure 6 page 3 paragraph [0031]).

Claims 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), and further in view of Meagher (US 5054020).

As per claim 10 Price discloses a SYNC pulse signal generated based on a predetermined temporal relationship between a first clock signal operable to clock a first circuit portion and a second clock signal operable to clock a second circuit portion (figure 8 column 2 lines 18-29 column 9 lines 37-42 and lines 65-67). Price doesn't disclose that when the signal contains a plurality of logic lows during a predetermined time period, inserting a logic high condition at a select point in time. It is very well known and Meagher discloses that when the signal contains a plurality of a logic lows during a predetermined time period, inserting a logic high condition at a select point in time (figure 2, column 2 lines 30-31). Price and Meagher teachings are from similar

problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate synchronization technique disclosed by Meagher with the SYNC pulse signal disclosed by Price. The suggestion/motivation for doing so would have been to prevent the lost of synchronization avoiding the use of a sequence of predetermined zeros (Meagher figure 2, column 2 lines 30-31).

As per claim 12 Price also discloses that the SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal (figures 13 and 14 point 1 column 14 line 62 to column 15 line 8).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), further in view of Meagher (US 5054020) and further in view of Langendorf (US 5256994). Price and Meagher disclose claim 10. Price and Meagher don't specifically disclose that the second clock signal is generated by a phase-locked loop (PLL) based on said first clock signal. It is very well known and Langendorf disclose the case where the second clock signal is generated by a phase-locked loop (PLL) based on said first clock signal (figure 2 column 5 lines 53-55). Price, Meagher and Langendorf teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the use of a PLL to generate the second clock signal as disclosed by and Langendorf with the SYNC pulse signal disclosed by Price and Meagher. The suggestion/motivation for doing so would have to provide synchronization between the two clock domains (Langendorf abstract).

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Price (US 5450458), further in view of Meagher (US 5054020) and further in view of Magro (US 6516362). Price and Meagher disclose claim 10. Price and Meagher don't specifically disclose that the SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal. Magro specifically discloses that SYNC pulse signal is generated when a rising edge in said first clock signal coincides with a rising edge in said second clock signal (figure 3-6 column 8 lines 25-33). Price, Meagher and Magro teachings are from similar problem area. At the time of the invention it would have been obvious to a person of ordinary skill in the art to integrate the generation of the SYNC signal when a rising edge in said first clock signal coincides with a rising edge in said second clock signal as disclosed by and Magro with the SYNC pulse signal disclosed by Price and Meagher. The suggestion/motivation for doing so would have to provide communication among multiple computer devices operating at different frequencies utilizing clock synchronization (Magro abstract).

Allowable Subject Matter

Claim 13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is (571) 272-3119. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad H. Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAT 1-4-2005

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